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EE 465 Lab 1

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**Verilog Coding and Test Bench for Simple Functions**

# Introduction

The purpose of this lab was to simulate a circuit using Verilog in Multisim. The desired outputs are shown in Figure 1 and the schematic view is shown in Figure 3. To get the proper delays, three output registers were used. The output was saved into oRESULTA or oRESULTB for one clock cycle before being added or assigned to oRESULT. The timescale was set to 10 ns to simulate a 50 MHz clock.



Figure 1: The required outputs are shown above for different values of iSEL.

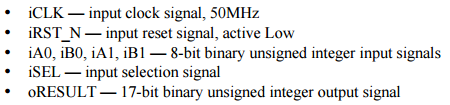


Figure 2: The variable parameters used in this lab are shown above.

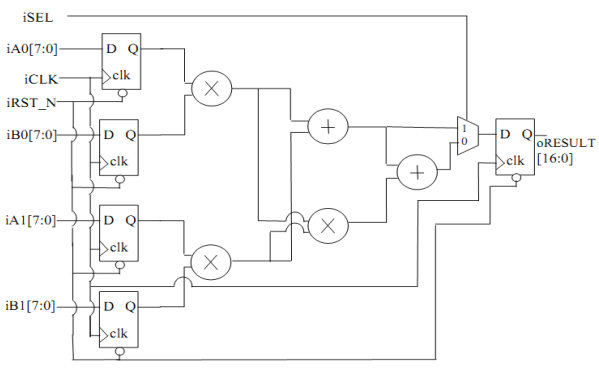


Figure 3: The schematic view of the required output is shown above.

# Module Code

module test(iCLK, iRST\_N, iSEL, iA0, iA1, iB0, iB1, oRESULT);

input iCLK, iRST\_N, iSEL, iA0, iA1, iB0, iB1;

output oRESULT;

wire iCLK, iRST\_N;

wire [7:0] iA0, iA1, iB0, iB1;

reg [16:0] oRESULTA, oRESULTB, oRESULT;

always @ (posedge iCLK)begin

if(iRST\_N)begin

oRESULTA <= iA0 \* iB0 + iA1 \* iB1;

oRESULTB <= iA0 \* iB0 + iA1 \* iB1 + iA0 \* iA1 \* iB0 \* iB1;

if(iSEL)begin

oRESULT <= oRESULTA ;

end

else begin

oRESULT <= oRESULTB;

end

end

else begin

oRESULT <= 0;

end

end

endmodule

# Testbench

`timescale 10ns/1ns

module test\_tb ();

reg iCLK\_t, iRST\_N\_t, iSEL\_t;

reg [7:0] iA0\_t, iA1\_t, iB0\_t, iB1\_t;

wire [16:0] oRESULT\_t;

test X(iCLK\_t, iRST\_N\_t, iSEL\_t, iA0\_t, iA1\_t, iB0\_t, iB1\_t, oRESULT\_t);

initial $display ("Test control");

initial $display ("%10s %10s %10s %10s %10s %10s %10s %10s",

"iCLK\_t", "iRST\_N\_t", "iSEL\_t", "iA0\_t", "iA1\_t",

"iB0\_t", "iB1\_t", "oRESULT\_t");

initial $monitor ("%10b %10b %10b %10d %10d %10d %10d %10d",

iCLK\_t, iRST\_N\_t, iSEL\_t, iA0\_t, iA1\_t, iB0\_t, iB1\_t, oRESULT\_t);

initial begin

iCLK\_t = 0;

iRST\_N\_t = 0;

iSEL\_t = 0;

iA0\_t = 0;

iA1\_t = 0;

iB0\_t = 0;

iB1\_t = 0;

#1

iRST\_N\_t = 1;

#3

iSEL\_t = 1;

iA0\_t = 2;

iA1\_t = 3;

iB0\_t = 5;

iB1\_t = 1;

#10

iSEL\_t = 0;

iA0\_t = 2;

iA1\_t = 3;

iB0\_t = 5;

iB1\_t = 1;

#10

iSEL\_t = 1;

iA0\_t = 2;

iA1\_t = 3;

iB0\_t = 5;

iB1\_t = 1;

#10

iSEL\_t = 0;

iA0\_t = 53;

iA1\_t = 26;

iB0\_t = 120;

iB1\_t = 5;

#10

iSEL\_t = 0;

iA0\_t = 26;

iA1\_t = 1;

iB0\_t = 15;

iB1\_t = 19;

#4

$stop;

end

always #1 iCLK\_t = ~iCLK\_t;

endmodule

Figure 4 shows that the output was delayed two clock cycles after a change was recorded for the inputs. The first result is iA0 \* iB0 + iA1 \* iB1 = 2\*5 +3\*1 = 13 because iSEL is high. The second result is after iSEL goes low and is iA0 \* iB0 + iA1 \* iB1 + iA0 \* iA1 \* iB0 \* iB1 = 13 + 2\*3\*5\*1 = 43.

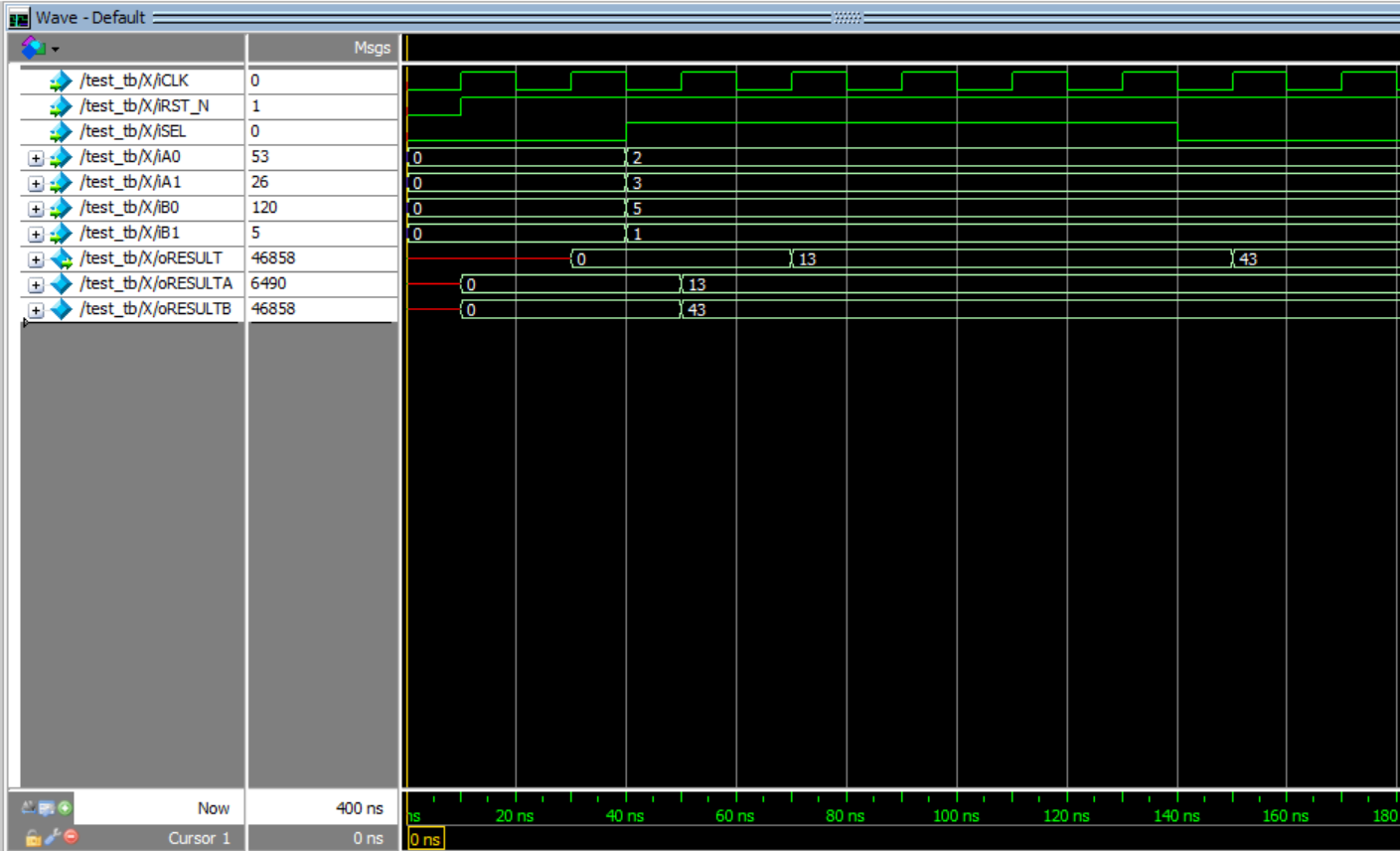


Figure 4: The wave view from the test bench output is shown above.

# Output

# 

Figure 5: The output values are shown above.

# Conclusion

This lab demonstrated how easy it is to go from concept to testing using Verilog. The only tricky part was getting the output to change with the correct delays to match the actual circuit output.